

## Application-Specific Information

# MPC7400 Part Number Specification

This document describes part number specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7400 Hardware Specifications*.

Specifications provided in this Part Number Specification supersede those in the *MPC7400 Hardware Specifications* dated 9/99 (order #: MPC7400EC/D) for these part numbers only; specifications not addressed herein are unchanged. This document is frequently updated, refer to the website at <http://www.mot.com/SPS/PowerPC/> for the latest version.

Note that headings and table numbers in this data sheet are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table A. For more detailed ordering information see Table B.

**Table A. Part Numbers Addressed by this Data Sheet**

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	Vdd	T <sub>J</sub> (°C)	
XPC7400RX400PK	400 MHz	2.15V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 400Mhz frequency
XPC7400RX450PK	450 MHz	2.15V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 450Mhz frequency
XPC7400RX500PK	500 MHz	2.15V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 500Mhz frequency

Note: The X prefix in a Motorola PowerPC part number designates a "Pilot Production Prototype" as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes

## Errata

This section summarizes design defects or errors (errata) that are known to exist for these parts. There may be additional errata that are not known or are not yet documented here which may cause the part to deviate from the functional description provided in the *MPC7400 RISC Microprocessor User's Manual* (order # MPC7400UM/AD Rev 0). Refer to the website at <http://www.mot.com/SPS/PowerPC/> for the latest version of this Part Number Specification or to your local Motorola sales office for later and/or more detailed description of the errata.

The known errata as of the date of this document are summarized below.

#	Problem	Description	Impact	Work-Around
1	Incorrect value was written to the MSR after running POR ABIST	When running ABIST after POR, the renames remained valid causing MSR to be updated with the incorrect value.	Running ABIST after POR	Insert an ISYNC instruction at the interrupt vector 0xFFFF0_0100

The PowerPC name and the PowerPC logotyp are trademarks of International Business Machines Corporation used by Motorola under license from International Business Machines Corporation.

This document contains information on a new product under development by Motorola. Motorola reserves the right to change or discontinue this product without notice.

© Motorola Inc. 1999. All rights reserved.

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**



**MOTOROLA**

#	Problem	Description	Impact	Work-Around
2	Not all GPRs and FPRs are initialized after ABIST	Not all GPRs and FPRs are initialized after ABIST due to invalid instructions in the instruction buffers.	GPRs and FPRs may not be initialized during ABIST if the contents of the instruction buffers can be decoded to non-zero GPR or FPR destination addresses.	None
3	Asserting TEA and ARTRY together may cause loss of data	Asserting TEA and ARTRY together in the first cycle of the snoop response window may cause loss of iside data.	Any system that permits the aggressive timing of TEA in the first cycle of the snoop response window.	Delay assertion of TEA until the second cycle of the snoop response window or later.
4	Incorrect condition code on mismatched LWARX/STWCX pair	A STWCX instruction may be performed without setting the condition code if the store hits in the L2 and the LWARX instruction that set the reservation is to another coherency granule.	Any code which uses mismatched LWARX/STWCX address pairs	1. Avoid mismatched LWARX/STWCX address pairs, or 2. Turn off the L2
5	TLBSYNC may hang in the presence of a DST	The MPC7400 may not make forward progress if a DST has caused an MMU tablewalk, that MMU tablewalk was marked by a TLBIE instruction, and a TLBSYNC instruction is pipelined the cycle after the MMU tablewalk accesses the dL1 cache.	Any system which has an active DST engine while executing a TLBSYNC instruction in a privileged context	Insert a DSSALL instruction before a TLBSYNC instruction
6	Queueing six transactions to secondary bus may hang the system	Queueing six transactions from a single MAX processor could use all Data Transaction Queue resources and hang the system if forward progress cannot be made by allowing MAX to complete at least one outstanding transaction.	Any system which allows 6 outstanding transactions from a single processor and which has a secondary bus with characteristics as detailed in full description.	1. Limit the number of outstanding transactions from a secondary bus to 5 in system logic, or 2. Mark the memory space on the secondary bus as guarded and avoid DST(ST)(T) and LMW instructions.

## 1.2 General

This section summarizes changes to the features of the MPC7400 described in the *MPC7400 Hardware Specifications*.

- None.

### 1.4.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7400 part numbers described herein.

**Table 3. Recommended Operating Conditions**

Characteristic	Symbol	Recommended Value	Unit
Core supply voltage	Vdd	2.15V±50mV	
PLL supply voltage	AVdd	2.15V±50mV	
L2 DLL supply voltage	L2AVdd	2.15V±50mV	

**Table 3. Recommended Operating Conditions (Continued)**

Characteristic		Symbol	Recommended Value	Unit
Processor bus supply voltage	BVSEL = 0	OVdd	1.8V±100mV	V
	BVSEL = $\overline{\text{HRESET}}$	OVdd	2.5V±100mV	V
	BVSEL = 1	OVdd	3.3V±165mV	V
L2 bus supply voltage	L2VSEL = 0	L2OVdd	1.8V±100mV	V
	L2VSEL = $\overline{\text{HRESET}}$	L2OVdd	2.5V±100mV	V
	L2VSEL = 1	L2OVdd	3.3V±165mV	V
Input voltage	Processor bus	V <sub>in</sub>	GND to OVdd	V
	L2 Bus	V <sub>in</sub>	GND to L2OVdd	V
	JTAG Signals	V <sub>in</sub>	GND to OVdd	V
Die-junction temperature		T <sub>j</sub>	0-65	°C

**Note:** These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 7 provides the power consumption for the MPC7400 part at the frequencies described herein.

**Table 7. Power Consumption for MPC7400**

	Processor (CPU) Frequency	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	450Mhz	500Mhz		
<b>Full-On Mode</b>					
Typical	7.56	8.51	9.45	W	1, 3
Maximum	15.1	17.0	18.9	W	1, 2, 4
<b>Doze Mode</b>					
Maximum	6.7	7.5	8.3	W	1, 2
<b>Nap Mode</b>					
Maximum	2.7	3.0	3.3	W	1, 2
<b>Sleep Mode</b>					
Maximum	2.7	3.0	3.3	W	1, 2
<b>Sleep Mode—PLL and DLL Disabled</b>					
Typical	600	600	600	mW	1, 3
Maximum	1.0	1.0	1.0	W	1, 2

**Notes:**

See General hardware specification

4. These values are with Altivec. Without Altivec, estimate a 25% decrease.

## 1.4.2.1 Clock AC Specifications

Table 8 provides the additional clock AC timing specifications described in this Part Number Specification. Refer to the MPC7400

Hardware Specification for the remaining frequencies.

**Table 8. Clock AC Timing Specifications**

At recommended operating conditions (See Table 3)

Characteristic	Symbol	400 MHz		450 MHz		500MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Processor frequency	$f_{core}$	350	400	350	450	350	500	MHz	
VCO frequency	$f_{VCO}$	700	800	700	900	700	1000	MHz	
SYSCLK frequency	$f_{SYSCLK}$	33	100	33	100	33	100	MHz	1
SYSCLK cycle time	$t_{SYSCLK}$	10	30	10	30	10	30	ns	
SYSCLK rise and fall time	$t_{KR} \& t_{KF}$	—	1.0	—	1.0	—	1.0	ns	2
		—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at $OV_{dd}/2$	$t_{KHL}/t_{SYSCLK}$	40	60	40	60	40	60	%	4
SYSCLK jitter		—	$\pm 150$	—	$\pm 150$	—	$\pm 150$	ps	5
Internal PLL relock time		—	100	—	100	—	100	$\mu s$	6
<b>Notes:</b> See General hardware specification.									

## 1.4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7400 part described in this Part Number Specification.

**Table 9. Processor Bus AC Timing Specifications<sup>1</sup>**

At  $V_{dd}=AV_{dd}=2.15V \pm 50mV$ ;  $0 \leq T_j \leq 65^\circ C$ ,  $OV_{dd} = 3.3V \pm 165mV$  or  $OV_{dd} = 2.5V \pm 100mV$  or  $OV_{dd}=1.8V \pm 100mV$

Parameter	Symbol	400, 450, 500 Mhz		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{HRESET}$	$t_{MVRH}$	8	—	$t_{sysclk}$	2,3,4,5
$\overline{HRESET}$ to mode select input hold	$t_{MXRH}$	0	—	ns	2,3,5
Setup Times:				ns	10
Address/Transfer Attribute	$t_{AVKH}$	1.4	—		6
Transfer Start (TS)	$t_{TSVKH}$	1.4	—		—
Data/Data Parity	$t_{DVKH}$	1.4	—		7
ARTRY/SHD0/SHD1	$t_{ARVKH}$	1.4	—		—
All Other Inputs	$t_{IVKH}$	1.4	—		8
Input Hold Times:				ns	11
Address/Transfer Attribute	$t_{AXKH}$	0	—		6
Transfer Start (TS)	$t_{TSXKH}$	0	—		—
Data/Data Parity	$t_{DXKH}$	0	—		7
ARTRY/SHD0/SHD1	$t_{ARXKH}$	0	—		—
All Other Inputs	$t_{IXKH}$	0	—		8
Valid Times:				ns	12
Address/Transfer Attribute	$t_{KHAV}$	—	3.0		6
TS, ABB, DBB	$t_{KHTSV}$	—	3.0		—
Data	$t_{KHDV}$	—	3.5		7
Data Parity	$t_{KHDPV}$	—	3.5		7
ARTRY/SHD0/SHD1	$t_{KHARV}$	—	2.3		—
All Other Outputs	$t_{KHOV}$	—	3.0		9
Output Hold Times:				ns	13
Address/Transfer Attribute	$t_{KHAX}$	0.75	—		6
TS, ABB, DBB	$t_{KHTSX}$	0.75	—		—
Data/Data Parity	$t_{KHDX}$	0.6	—		7
ARTRY/SHD0/SHD1	$t_{KHARX}$	0.75	—		—
All Other Outputs	$t_{KHOX}$	0.75	—		9

## Table 9. Processor Bus AC Timing Specifications<sup>1</sup> (Continued)

At Vdd=AVdd=2.15V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 3.3V±165mV or OVdd = 2.5V±100mV or OVdd=1.8V±100mV

Parameter	Symbol	400, 450, 500 Mhz		Unit	Notes
		Min	Max		
SYSCLK to Output Enable	t <sub>KHOE</sub>	0.5	—	ns	14
SYSCLK to Output High Impedance (all except TS, ABB/AMON(0), ARTRY/SHD, DBB/DMON(0))	t <sub>KHOZ</sub>	—	3.5	ns	15
SYSCLK to TS, ABB/AMON(0), DBB/DMON(0) High Impedance after precharge	t <sub>KHABPZ</sub>	—	1.0	t <sub>sysclk</sub>	4,15, 16,17
Maximum Delay to ARTRY/SHD0/SHD1 Precharge	t <sub>KHARP</sub>	—	1	t <sub>sysclk</sub>	4,17
SYSCLK to ARTRY/SHD0/SHD1 High Impedance After Precharge	t <sub>KHARPZ</sub>	—	2	t <sub>sysclk</sub>	4,17

### Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mW and L2AVdd = 15 mW.
2. Maximum power is measured at Vdd = 2.2V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including Altivec, maximally busy.
3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 2.15V, OVdd = L2OVdd = 3.3V in a system while running a codec application that is Altivec intensive.

### 1.4.2.3 L2 Clock AC Specifications

Table 10 provides the L2CLK Output AC Timing Specifications for the MPC7400 part described in this Part Number Specification.

## Table 10. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK frequency	f <sub>L2CLK</sub>	150	400	150	450	150	500	MHz	1
L2CLK cycle time	t <sub>L2CLK</sub>	2.5	6.67	2.22	6.67	2.0	6.67	ns	
L2CLK duty cycle	t <sub>CHCL</sub> /t <sub>L2CLK</sub>	50		50		50		%	2
Internal DLL-relock time		640	—	640	—	640	—	L2CLK	4
DLL capture window			±200		±200		±200	ns	5
<b>Notes:</b> See General hardware specification.									

## 1.4.2.4 L2 Bus AC Specifications

Table 11 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this Part Number Specification.

**Table 11. L2 Bus Interface AC Timing Specifications**

At Vdd=AVdd=L2AVdd= 2.15V±50mV; 0 ≤ Tj ≤ 65°C, L2OVdd = 3.3V±165mV or L2OVdd = 2.5V±100mV or L2OVdd=1.8V±100mV

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2SYNC_IN rise and fall time	t <sub>L2CR</sub> & t <sub>L2CF</sub>	—	1.0	—	1.0	—	1.0	ns	1
Setup Times: Data and parity	t <sub>DVL2CH</sub>	1.5	—	1.3	—	1.0	—	ns	2
Input Hold Times: Data and parity	t <sub>DXL2CH</sub>	—	0.0	—	0.0	—	0.0	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t <sub>L2CHOV</sub>	- - - -	2.5 3.0 3.5 4.0	- - - -	2.4 - - -	- - - -	2.3 - - -	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t <sub>L2CHOX</sub>	0.4 1.0 1.4 1.8	- - - -	0.3 - - -	- - - -	0.2 - - -	- - - -	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t <sub>L2CHOZ</sub>	- - - -	2.0 2.5 3.0 3.5	- - - -	2.0 2.5 3.0 3.5	- - - -	2.0 2.5 3.0 3.5	ns	
<b>Notes:</b> See General Hardware Specification									

## 1.10 Ordering Information

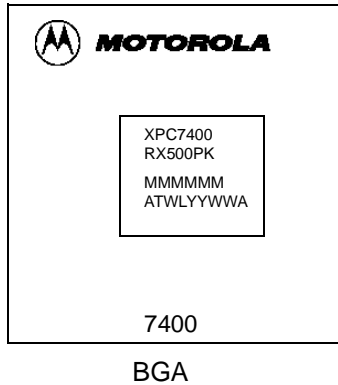
Table B provides the ordering information for the MPC7400 part described in this Part Number Specification..

**Table B. Ordering Information for the MPC7400 Microprocessor**

Package Type	Device Rev	Process	Mask Code	CPU Frequency (MHz)	Motorola Part Number
360 CBGA	2.9	HIP5P	89J87W or 89K62D	400MHz	XPC7400RX400PK
				450MHz	XPC7400RX450PK
				500MHz	XPC7400RX500PK

### 1.10.1 Part Marking

Parts are marked as the example shown in Figure A.



**Notes:**

MMMMMM is the 6-digit mask number

ATWLYYWWA is the traceability code


CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

**Figure A. Motorola Part Marking for BGA Device**

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC.

Information in this document is provided solely to enable system and software implementers to use PowerPC microprocessors. There are no express or implied copyright licenses granted hereunder to design or fabricate PowerPC integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

IBM is a registered trademark of International Business Machines Corporation.

The PowerPC name and the PowerPC logotype are trademarks of International Business Machines Corporation used by Motorola under license from International Business Machines Corporation. International Business Machines Corporation is an Equal Opportunity/Affirmative Action Employer.

